03-24-00

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LIMBACH & LIMBACH L.L.P.
2001 Ferry Building, San Francisco, CA 94111
415/433-4150

Address to:
Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney's Docket No. NSC1-G390
[P04493]
First Named Inventor MATTHEW DOUGLAS PE

UTILITY PATENT APPLICATION TRANSMITTAL
(under 37 CFR 1.53(b))

SIR:

Transmitted herewith for filing is the patent application entitled:
SILICON-BACKED MICRODISPLAY WITH A GLASS-SIDE PASSIVATION LAYER

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date March 23, 2000, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EL254109868US addressed to: Box Patent Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

JOHN LYDDAN
(Name of person mailing paper)

John Lyddan
(Signature)

Enclosed are:

1. X Transmittal Form (two copies required)

2. The papers required for filing date under CFR § 1.53(b):
   i. 11 Pages of specification (including claims and abstract);
   ii. 1 Sheets of drawings.
   __ formal x informal

3. Declaration or oath

   a. x Newly executed (original or copy)

4. __ Microfiche Computer Program (Appendix, see 37 CFR 1.96)

5. __ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
   i. __ Computer Readable Copy
   ii. __ Paper Copy (identical to computer copy)
   iii. __ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

6. __ An assignment of the invention to NATIONAL SEMICONDUCTOR CORPORATION is attached (including Form PTO-1595).

   i. __ 37 CFR 3.73(b) Statement (when there is an assignee)

7. __ Power of Attorney

8. __ An Information Disclosure Statement (IDS) is enclosed, including a PTO-1449 and copies of __ references.

9. __ Preliminary Amendment.

10. X Return Receipt Postcard (MPEP 503 -- should be specifically itemized)

11. __ Other

12. FOREIGN PRIORITY
[] Priority of application no. _ filed on _ in _ is claimed under 35 USC 119.

The certified copy of the priority application:
- _ is filed herewith; or
- _ has been filed in prior application no. NEW filed on HEREWITH, or
- _ will be provided.

__ English Translation Document (if applicable)

13. **FEE CALCULATION**

a. __ Amendment changing number of claims or deleting multiple dependencies is enclosed.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee ($690)
Total Claims	15 - 20	* 0	x $18.00	0
Independent Claims	2 - 3	* 0	x $78.00	0
__ Multiple dependent claim(s), if any			$260.00	0

*If less than zero, enter "0".

Filing Fee Calculation $690

50% Filing Fee Reduction (if applicable) . . . . . $

14. Small Entity Status
a. __ A small entity statement is enclosed.
b. __ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
c. __ is no longer claimed.

15. Other Fees
__ Recording Assignment [$40.00] . . . . . $
__ Other fees
Specify _____ . . . . . $

Total Fees Enclosed $690

16. Payment of Fees
x Check(s) in the amount of $ 690 enclosed.
__ Charge Account No. 12-1420 in the amount of $__.
A duplicate of this transmittal is attached.

17. All correspondence regarding this application should be forwarded to the undersigned attorney:

Mayumi Maeda
Limbach & Limbach L.L.P.
2001 Ferry Building
San Francisco, CA 94111
Telephone: 415/433-4150
Facsimile: 415/433-8716

18. Authorization to Charge Additional Fees

X The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 12-1420. **A duplicate of this transmittal is attached**.

LIMBACH & LIMBACH L.L.P.

March 23, 2000
(Date)

By: _____
Mayumi Maeda
Registration No. 40,075
Attorney(s) or Agent(s) of Record

Attorney Docket No. NSC1-G3900
[P04391]

PATENT

SILICON-BACKED MICRODISPLAY WITH A GLASS-SIDE PASSIVATION LAYER

INVENTORS: Matthew Douglas Penry and Russell Flack

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to liquid crystal displays and, in particular, to silicon-backed microdisplays.

2. Description of the Related Art

Conventional liquid crystal displays (LCDs) include two sheets of glass arranged to form a thin cell, which is filled with a liquid crystal material. One of the sheets of glass includes transistors and pixel activation plates on its surface that serve to activate the liquid crystal material at discrete pixel locations. See U.S. Patent 5,299,289 to Omae et al. for a description of conventional LCDs. A silicon-backed microdisplay is essentially a miniaturized LCD with a silicon die substituted for one of the glass sheets. The surface of the silicon die includes the transistors (typically CMOS-based), pixel activation plates, and drive circuitry (e.g. row and column drivers) required for operation of the silicon-backed microdisplay. The pixel activation plates also serve as reflector plates that reflect incoming light back towards a viewer during operation of the silicon-backed microdisplay.

A portion of a representative silicon-backed microdisplay is shown in cross-section in FIG. 1. Silicon-backed microdisplay portion 10 includes a silicon die 12, a silicon-side conductive layer 14 disposed on the silicon die 12, and a silicon-side passivation layer 16 disposed on the silicon-side conductive layer 14. Silicon-backed microdisplay portion 10 also includes a cover glass 18, and glass-side conductive layer 20 disposed on the bottom surface of the cover glass 18. As shown in FIG. 1, a uniform gap is present between the silicon-side

passivation layer 16 and the glass-side conductive layer 20. This gap is filled with liquid crystal material 22. The combination of silicon die 12, silicon-side conductive layer 14, silicon-side passivation layer 16, cover glass 18, glass-side conductive layer 20 and liquid crystal material 22 essentially constitutes a miniature reflective mode, silicon-backed microdisplay.

To change the orientation of the liquid crystal material 22 and, therefore, affect the amount of light passing through the liquid crystal material 22, an AC electrical bias is applied between the silicon die 12 and the cover glass 18. Due to the electrical and surface properties of the cover glass 18, glass-side conductive layer 20, silicon-side passivation layer 16, silicon-side conductive layer 14 and silicon die 12, however, the microdisplay can exhibit flicker during operation. Such flicker, if visible to a user, renders the silicon-backed microdisplay unfit for commercial sale.

U.S. Patent 5,764,324 to Lu et al. (hereinafter the '324 patent), which is hereby incorporated by reference, utilizes additional films coated on the silicon-side conductive layer to reduce flicker. The types of additional films which can be commercially applied on the silicon-side of a silicon-backed microdisplay are, however, limited by the nature of the silicon-side conductive layer, as well as by the need to provide predetermined transmissive and reflective optical properties on the silicon-side of the silicon-backed microdisplay. The approach described in the '324 patent, therefore, may not be capable of adequately reducing flicker. In addition, in the microdisplay described in the '324 patent, the glass-side conductive layer is uncoated, thereby allowing various impurities from subsequent processes to modify its surface properties (e.g., work function) in an uncontrolled manner.

Still needed in the field, therefore, is a silicon-backed microdisplay that provides for reduced flicker and also provides for the protection of its glass-side conductive layer during subsequent processing.

SUMMARY OF THE INVENTION

The present invention provides a silicon-backed microdisplay with reduced flicker and a glass-side conductive layer that is protected during subsequent processing. Silicon-backed microdisplays according to the present invention includes a silicon die, a silicon-side conductive layer disposed on the silicon die, and a silicon-side passivation layer disposed on the silicon-side conductive layer. The silicon-baked microdisplay also includes a cover glass, a glass-side conductive layer disposed on the cover glass and a glass-side passivation layer of a predetermined material and thickness disposed on the glass-side conductive layer. Furthermore, liquid crystal material is sandwiched between the glass-side passivation layer and the silicon-side passivation layer in silicon-backed microdisplays according to the present invention.

Visible flicker is suppressed in silicon-backed microdisplays according to the present invention by selecting a glass-side passivation layer material and thickness that improve the work function balance between (i) a combination (i.e. aggregate) of the glass-side conductive layer and the glass-side passivation layer and (ii) a combination (i.e. aggregate) of the silicon-side passivation layer and the silicon-side conductive layer. The glass-side passivation layer materials include, but are not necessarily limited to, CeO_2, In_2O_3, MgO, SnO_2, Ta_2O_5, TiO_2, Y_2O_3, ZnO, SiO_2, Al_2O_3, BeO and MgF_2. Although the appropriate glass-side passivation layer thickness depends upon the degree of work function balance improvement desired, a typical thickness is in the range of 300 angstroms to 900 angstroms. The presence of a glass-side passivation layer also helps maintain the work function balance by protecting the glass-side conductive layer surface from exposure to impurities.

BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description that

sets forth illustrative embodiments, in which the principles of the invention are utilized, and the accompanying drawings, of which:

FIG. 1 is a cross-sectional representation of a portion of a conventional silicon-backed microdisplay.

FIG. 2 is a cross-sectional representation of a portion of a silicon-backed microdisplay in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

A portion of a representative silicon-backed microdisplay 30 according to the present invention is illustrated in cross-section in FIG. 2. Silicon-backed microdisplay portion 30 includes a silicon die 32, a silicon-side conductive layer 34 disposed on the silicon die 32, and a silicon-side passivation layer 36 disposed on the silicon-side conductive layer 34. Silicon-backed microdisplay portion 30 also includes a cover glass 38, a glass-side conductive layer 40 disposed on the bottom surface of the cover glass 38 and a glass-side passivation layer 44 disposed on the glass-side conductive layer 40. A uniform gap between the silicon-side passivation layer 36 and the glass-side passivation layer 44 is filled with liquid crystal material 42.

Silicon-side conductor layer 34 can be a conventional silicon-side conductive layer, such as an aluminum layer, produced during fabrication of silicon die 32. Silicon-side passivation layer 36 typically includes a silicon dioxide (SiO_2) layer in combination with silicon nitride (Si_3N_4) layer, and is formed using methods well known to one skilled in the art. The total thickness of the silicon-side passivation layer 36 is typically in the range of 2,000 angstroms to 6,000 angstroms.

Cover glass 38 can be produced from commercially available cover glass material, such as optical-grade, borosilicate glass manufactured by Corning. A typical thickness range for the cover glass 38 is 0.5mm to 1.1mm. Glass-side conductive layer 40 is typically formed of a material that includes indium-tin-oxide (ITO), has a characteristic resistance in the range of 100 ohms/square to

500 ohms/square, and a light transmissivity of 90% or greater. The glass-side conductive layer 40 can be formed on the cover glass 38 using, for example, evaporative or sputtering techniques well known in the art. Liquid crystal material 42 is a commercially available mixture whose composition is proprietary to the various commercial suppliers.

The material and thickness of the glass-side passivation layer 44 are predetermined to improve the work function balance between (i) the combination (i.e. aggregate) of the glass-side passivation layer and the glass side conductive layer and (ii) the combination (i.e. aggregate) of the silicon-side passivation layer and the silicon-side conductive layer. Therefore, the glass-side passivation layer 44 must be of a material and a thickness that will beneficially affect the work function of the glass-side conductive layer 40 when combined with that layer. For example, if the combination of the silicon-side passivation layer and the silicon-side conductive layer has a work function of 4.5 eV, and if the glass-side conductive layer alone has a work function of 4.8 eV, then a glass-side passivation layer material and thickness are selected so that the work function for the combination of the glass-side passivation layer and the glass-side conductive layer becomes closer to 4.5 eV than 4.8 eV. In other words, the objective is to use the glass-side passivation layer to modify the work function of the glass-side conductive layer in such a manner that the work function of the combination of the glass-side conductive layer and the glass-side passivation layer is close enough to the work function of the combination of the silicon-side passivation layer and the silicon-side conductive layer that the flicker is no longer visible.

Exemplary materials from which a selection can be made for the glass-side passivation layer 44, and their estimated work functions (listed in parenthesis), include CeO_2 (4.021 eV), In_2O_3 (3.946 eV), MgF_2 (4.102 eV), MgO (4.102 eV), SnO_2 (4.145 eV), Ta_2O_5 (4.153 eV), TiO_2 (4.323 eV), Y_2O_3 (3.776 eV), ZnO (3.814 eV), SiO_2 3.983 eV, Al_2O_3 (alumina, 4.442 eV) and BeO (4.480 eV).

It is preferred that the glass-side passivation layer thickness be thin enough that an electrical bias applied between the silicon die and the cover glass is not noticeably affected. A typical thickness for the glass-side passivation layer 44 in silicon-backed microdisplays according to the present invention is in the range of 300 angstroms to 900 angstroms. It is also preferred that the selection of a glass-side passivation layer material and thickness result in a combination of the glass-side passivation layer and the glass side conductive layer with an overall transmissivity of greater than 90% and a reflectivity of less than 1%.

It is believed that visible flicker in silicon-backed microdisplays is due, at least in part, to differences in the electrical characteristics (for example, the electromotive force, the ability to gather and give-off electrons) of the silicon-side conductive layer surface and the glass-side conductive layer surface. Visible flicker is, therefore, related to each of these surfaces' work function and to the difference between the respective work functions (i.e., the work function balance).

Moreover, the inventors have established that an improved work function balance (i.e., reducing the difference in the work functions) between the combination of the glass-side conductive layer and the glass-side passivation layer and the combination of the silicon-side conductive layer and the silicon-side passivation layer will reduce visible flicker in a silicon-backed microdisplay. This reduction in visible flicker was established using light meter-based, quantitative flicker measurements of silicon-backed microdisplays according to the present invention operated under controlled conditions.

The work functions for various materials are typically estimated using blocks of material measured in a vacuum. However, relatively thin layers of materials that are disposed on other materials inherently behave differently from blocks of material, since the relatively thin layers are influenced by what is on top of them and what is underneath them. In addition, work functions are very difficult to measure since the conventional measurement techniques often produce more measurement error than the small differences in work function

that are of interest. Therefore, measurements of the actual work function balance for silicon-backed microdisplays according to the present invention are not readily made. It is believed, however, that the work function balance for a conventional silicon-backed microdisplay is in the range of approximately 0.3 eV to 0.5 eV. And, it is postulated, without being bound, that silicon-backed microdisplays according to the present invention improve the conventional work function balance by at least 0.1 eV to 0.2 eV.

Glass-side conductive layers, such as those formed of indium-tin-oxide (ITO), can be easily oxidized or etched by other chemicals or impurities, including those that are used in the manufacture of microdisplays or are present in the liquid crystal material. In addition to improving work function balance, the glass-side passivation layers of the present invention provide the benefit of protecting the glass-side conductive layer surface from uncontrolled modification due to exposure to chemicals or impurities during manufacture or operation of the silicon-backed microdisplay.

It should be understood that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and that structures within the scope of these claims and their equivalents be covered thereby.

WHAT IS CLAIMED IS:

1. A silicon-backed microdisplay comprising:

a silicon die;

a silicon-side conductive layer disposed on the silicon die;

a silicon-side passivation layer disposed on the silicon-side conductive layer;

a cover glass;

a glass-side conductive layer disposed on the cover glass;

a glass-side passivation layer of a predetermined material and thickness disposed on the glass-side conductive layer; and

liquid crystal material sandwiched between the glass-side passivation layer and the silicon-side passivation layer;

wherein the thickness and material of the glass-side passivation layer are predetermined to improve the work function balance between a combination of the glass-side conductive layer and the glass-side passivation layer and a combination of the silicon-side passivation layer and the silicon-side conductive layer,

thereby providing a silicon-backed microdisplay with reduced visible flicker.

2. The silicon-backed microdisplay of claim 1 wherein the silicon-side conductive layer is formed of aluminum, the silicon-side passivation layer is formed of silicon dioxide and silicon nitride, and the glass-side conductive layer is formed of indium-tin-oxide.

3. The silicon-backed microdisplay of claim 2 wherein the glass-side passivation layer includes SiO_2.

4. The silicon-backed microdisplay of claim 2 wherein the glass-side passivation layer includes Al_2O_3.

5. The silicon-backed microdisplay of claim 2 wherein the glass-side passivation layer includes BeO.

6. The silicon-backed microdisplay of claim 2 wherein the glass-side passivation layer includes MgF_2.

7. The silicon-backed microdisplay of claim 2 wherein the glass-side passivation layer material includes a material selected from the oxide material group consisting of CeO_2, In_2O_3, MgO, SnO_2, Ta_2O_5, TiO_2, Y_2O_3, ZnO, and any combinations thereof.

8. The silicon-backed microdisplay of claim 1 wherein the predetermined thickness of the glass-side passivation layer is in the range of 300 angstroms to 900 angstroms.

9. The silicon-backed microdisplay of claim 1 wherein the work function balance is less than 0.5 eV.

10. The silicon-backed microdisplay of claim 1 wherein the work function balance is less than 0.3 eV.

11. The silicon-backed microdisplay of claim 1 wherein the glass-side passivation layer improves the work function balance by at least 0.1 eV.

12. A silicon-backed microdisplay comprising:

a silicon die;

a silicon-side conductive layer formed of aluminum disposed on the silicon die;

a silicon-side passivation layer formed of silicon dioxide and silicon nitride, the silicon-side passivation layer disposed on the silicon-side conductive layer;

a cover glass;

a glass-side conductive layer formed of indium-tin-oxide disposed on the cover glass;

a glass-side passivation layer disposed on the glass-side conductive layer; and

liquid crystal material sandwiched between the glass-side passivation layer and the silicon-side passivation layer;

wherein the thickness and material of the glass-side passivation layer are predetermined to improve the work function balance between a combination of the glass-side conductive layer and the glass-side passivation layer and a combination of the silicon-side passivation layer and the silicon-side conductive layer,

thereby providing a silicon-backed microdisplay with reduced visible flicker.

13. The silicon-backed microdisplay of claim 12 wherein the glass-side passivation layer includes SiO_2.

14. The silicon-backed microdisplay of claim 12 wherein the glass-side passivation layer includes Al_2O_3.

15. The silicon-backed microdisplay of claim 12 wherein the glass-side passivation layer includes BeO.

ABSTRACT OF THE DISCLOSURE

A silicon-backed microdisplay with reduced flicker and a protected glass-side conductive layer. The silicon-backed microdisplay includes a silicon die, a silicon-side conductive layer disposed on the silicon die, and a silicon-side passivation layer arranged on the silicon-side conductive layer. The silicon-backed microdisplay also includes a cover glass, a glass-side conductive layer disposed on the cover glass and a glass-side passivation layer of a predetermined material and thickness arranged on the glass-side conductive layer. Liquid crystal material is sandwiched between the glass-side passivation layer and the silicon-side passivation layer in the silicon-backed microdisplay. Visible flicker is suppressed in the microdisplay by selecting a glass-side passivation layer material (for example, CeO_2, In_2O_3, MgO, SnO_2, Ta_2O_5, TiO_2, Y_2O_3, ZnO, SiO_2, Al_2O_3, BeO or MgF_2) and thickness (for example, in the range of 300 angstroms to 900 angstroms) that improve the work function balance between (i) a combination of the glass-side conductive layer and the glass-side passivation layer and (ii) a combination of the silicon-side passivation layer and the silicon-side conductive layer. The presence of a glass-side passivation layer will also help maintain the work function balance by protecting the glass-side conductive layer surface from exposure to impurities.

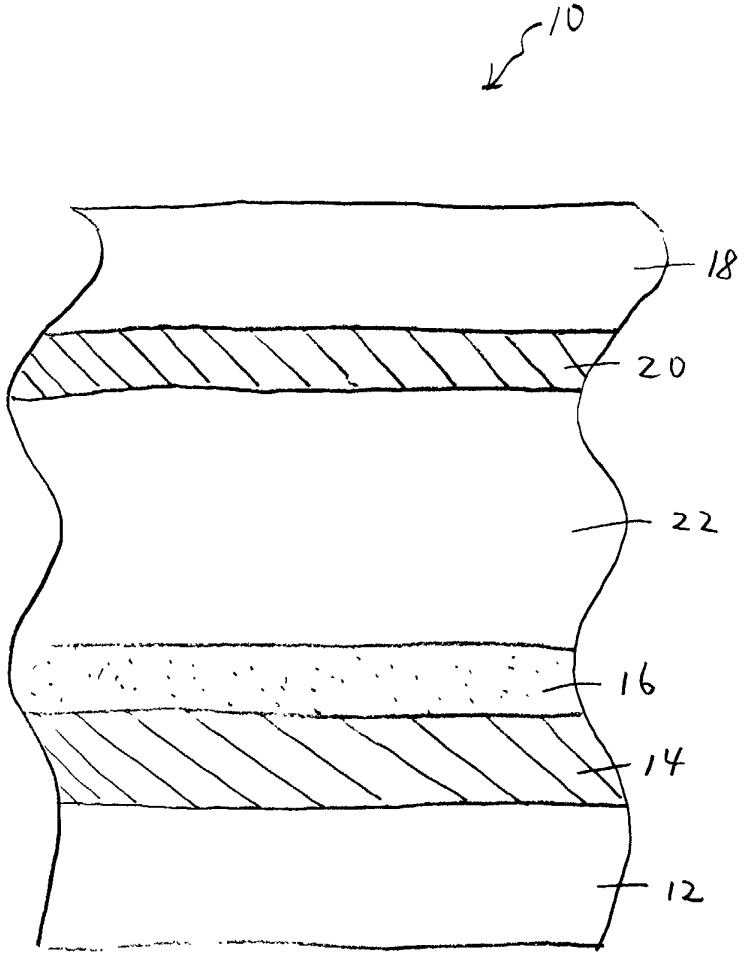

FIG. 1
PRIOR ART

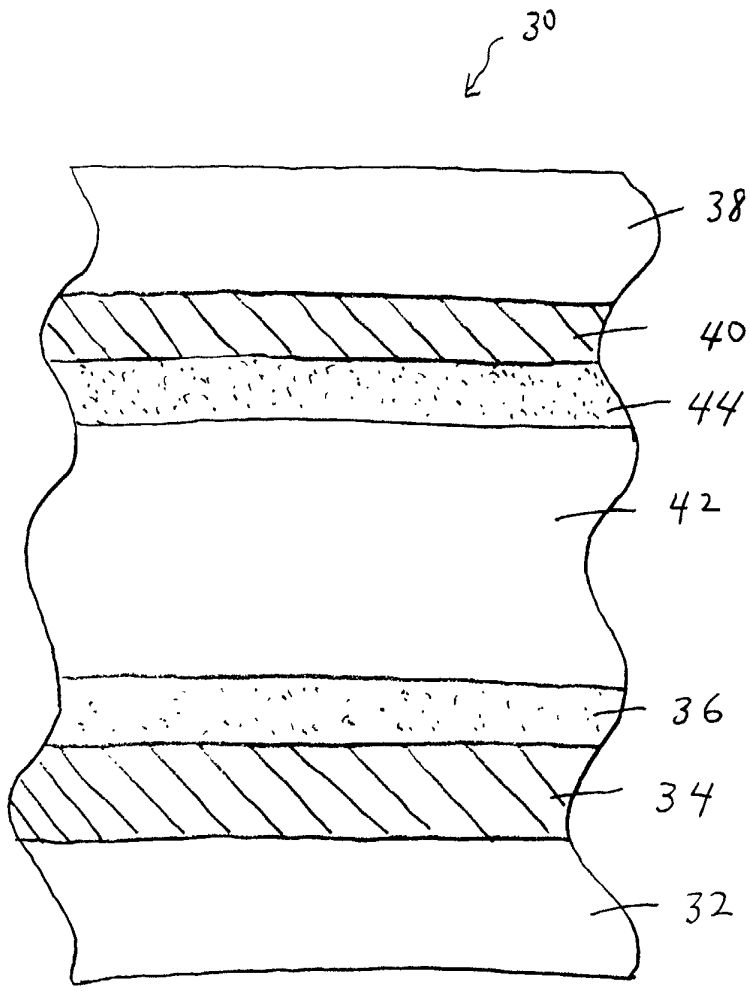

FIG. 2

Atty Docket No. NSC1-G3900 [P04391]

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SILICON-BACKED MICRODISPLAY WITH A GLASS-SIDE PASSIVATION LAYER

the specification of which (check one) __x__ is attached hereto or ___ was filed on ____ as Application No. ___ and was amended on ____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
			Yes	No
Number	Country	Day/Month/Year Filed	____	____

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) below.

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status: Patented, Pending, Abandoned
Application Number	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor MATTHEW DOUGLAS PENRY

Inventor's signature Matthew D. Penry 03-23-00
Date

Residence 1170 CASTLE LAKE CIRCLE, MORGAN HILL, CA 95037

Citizenship USA

Post Office Address 1170 CASTLE LAKE CIRCLE, MORGAN HILL, CA 95037

Full name of second joint inventor, if any, RUSSELL FLACK

Inventor's signature _____
Date

Residence 18920 ALCOTT WAY, SARATOGA, CA

Citizenship BRITISH

Post Office Address 18920 ALCOTT WAY, SARATOGA, CA

Full name of third joint inventor, if any, _____

Inventor's signature _____
Date

Residence _____

Citizenship _____

Post Office Address _____

Full name of fourth joint inventor, if any, _____

Inventor's signature _____
Date

Residence _____

Citizenship